Status of the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Previously Presented) A programmable gain amplifier, comprising:

a first buffer amplifier coupled between an input and an output, said first buffer amplifier controlled by a first switch;

a first resistor having a first terminal and a second terminal, said first terminal coupled to said input;

a second buffer amplifier coupled between said second terminal and said output, said second buffer amplifier controlled by a second switch; and

a second resistor having a third terminal and a fourth terminal, said third terminal coupled to said second terminal, said fourth terminal coupled to a ground.

20. (Previously Presented) The programmable gain amplifier of claim 19, wherein said first buffer amplifier is a transistor.

21. (Previously Presented) The programmable gain amplifier of claim 20, wherein said transistor is a metal oxide semiconductor field effect transistor.

22. (Previously Presented) The programmable gain amplifier of claim 21, wherein a gate terminal of said metal oxide semiconductor field effect transistor is coupled to said input.

23. (Previously Presented) The programmable gain amplifier of claim 22, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said output and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to said first switch.

24. (Previously Presented) The programmable gain amplifier of claim 22, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said first switch and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to a power supply voltage.

25. (Previously Presented) The programmable gain amplifier of claim 19, wherein said first switch is a transistor.

26. (Previously Presented) The programmable gain amplifier of claim 25, wherein said transistor is a metal oxide semiconductor field effect transistor.

27. (Previously Presented) The programmable gain amplifier of claim 26, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said first buffer amplifier and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to a power supply voltage.

28. (Previously Presented) The programmable gain amplifier of claim 26, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said output and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to said first buffer amplifier.

29. (Previously Presented) The programmable gain amplifier of claim 19, wherein said second buffer amplifier is a transistor.

30. (Previously Presented) The programmable gain amplifier of claim 29, wherein said transistor is a metal oxide semiconductor field effect transistor.

31. (Previously Presented) The programmable gain amplifier of claim 30, wherein a gate terminal of said metal oxide semiconductor field effect transistor is coupled to said second terminal.

32. (Previously Presented) The programmable gain amplifier of claim 31, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said output and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to said second switch.

33. (Previously Presented) The programmable gain amplifier of claim 31, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said second switch and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to a power supply voltage.

34. (Previously Presented) The programmable gain amplifier of claim 19, wherein said second switch is a transistor.

35. (Previously Presented) The programmable gain amplifier of claim 34, wherein said transistor is a metal oxide semiconductor field effect transistor.

36. (Previously Presented) The programmable gain amplifier of claim 35, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said second buffer amplifier and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to a power supply voltage.

37. (Previously Presented) The programmable gain amplifier of claim 35, wherein a source terminal of said metal oxide semiconductor field effect transistor is coupled to said

output and a drain terminal of said metal oxide semiconductor field effect transistor is coupled to said second buffer amplifier.

38. (Previously Presented) The programmable gain amplifier of claim 19, further comprising a bias voltage coupled between said fourth terminal and said ground.

39. (Previously Presented) The programmable gain amplifier of claim 19, further comprising a current source coupled between said output and said ground.

40. (Previously Presented) A programmable gain amplifier, comprising:

a first semiconductor device capable of coupling a signal from an input of the programmable gain amplifier to an output of the programmable gain amplifier;

a first resistor having a first terminal and a second terminal, said first terminal coupled to said input;

a second semiconductor device capable of coupling said signal from said second terminal to said output; and

a second resistor having a third terminal and a fourth terminal, said third terminal coupled to said second terminal, said fourth terminal coupled to a ground;

wherein when said signal has a voltage with a first absolute value larger than a second absolute value of a power supply voltage and said first semiconductor device is in an off state, said first semiconductor device remains in said off state.

41. (Previously Presented) A method for providing programmable amplification of a voltage signal, comprising the steps of:

(1) conveying the voltage signal along at least two parallel paths;

(2) attenuating the voltage signal along at least one of the at least two parallel paths to at least one fraction of the voltage signal;

(3) determining a desired fraction of the voltage signal; and

(4) activating an amplifier disposed within one of the at least two parallel paths that corresponds to the desired fraction of the voltage signal.